What is claimed:

1. A method of manufacturing a semiconductor device, comprising:

a laminating step including forming tunnel insulating films, floating gates, dielectric films and control gates on first and second cell areas, the first and second cell areas being formed mutually adjacent to each other on a semiconductor substrate; and

a plurality of impurity area formation steps for forming sources and drains on the first and second cell areas, and forming an electric connection between one of the source and drain of the first cell area on one hand and one of the source and drain of the second cell area on the other;

wherein a connecting area is formed as having a lower electric resistance than impurity areas formed in one of the plurality of impurity area formation steps.

2. The method of manufacturing a semiconductor device according to claim 1, wherein during the laminating step, a groove is formed on the connecting area on the surface of the semiconductor device.

3. The method of manufacturing a semiconductor device according to claim 2, wherein the laminating step comprises:

forming a first insulating film on the surface of the semiconductor substrate;

forming a first electrically conductive film on the first insulating film, etching the first electrically conductive film corresponding to the first and second cell areas, thereby partially exposing the first insulating film in a groove formation area;

forming a second insulating film on the exposed portions of the first insulating film and on the first electrically conductive film;

forming a second electrically conductive film on the second insulating film;

etching the second electrically conductive film corresponding to the control gates;

etching the second insulating film corresponding to the dielectric film, and etching, in the groove formation area, the first insulating film to partially expose the surface of the semiconductor substrate;

etching the first electrically conductive film corresponding to the floating gates, and etching the exposed portions of the surface of the semiconductor substrate so as to form the groove.

4. The method of manufacturing a semiconductor device according to claim 1, wherein the plurality of impurity area formation steps comprises injecting a first impurity into an area containing the connecting area, and injecting a second impurity into an area for the formation of source and drain of the first and second cell areas.

5. The method of manufacturing a semiconductor device according to claim 4, wherein the first impurity is injected with a patterned resist serving as a mask, and the second impurity is injected with the control gates, the dielectric films and the floating gates serving as masks.

6. The method of manufacturing a semiconductor device according to claim 4, wherein the first impurity is injected from an end portion of an area directly under the floating gate of the first cell area to a portion in front of an area directly under the floating gate of the second cell area.

7. The method of manufacturing a semiconductor device according to claim 4, wherein the first impurity is injected in an area away from an area directly under the floating gates of the first and second cell areas.

8. The method of manufacturing a semiconductor device according to claim 4, wherein the first impurity is injected into an area containing an end portion of an area directly under the floating gates of the first and second cell areas.

9. The method of manufacturing a semiconductor device according to claim 4, wherein a dosing amount of the first impurity is higher than a dosing amount of the second impurity.

10. The method of manufacturing a semiconductor device according to claim 4, wherein the first and second impurities are injected with the use of an ion injection technique, and an energy for injecting the first impurity is larger than an energy for injecting the second impurity.

11. The method of manufacturing a semiconductor device according to claim 4, wherein injecting the first impurity is carried out at the same time when forming one of a source/drain area and an off-set area of MOS transistor forming a surrounding circuit of the first and second memory cell areas.

12. The method of manufacturing a semiconductor device according to claim 1, wherein:

the connecting area is formed close to one of the source and drain of the first cell area, and also close to one of the source and drain of the second area; and

the plurality of the impurity area formation steps comprises:

injecting the first impurity into a source and drain formation area of the first cell area and into the connecting area; and

injecting the second impurity into a source and drain formation area of the second cell area and into the connecting area.

13. A semiconductor device comprising:

tunnel insulating films, floating gates, dielectric films and control gates, all of which are laminated on first and second cell areas on a semiconductor substrate;

sources and drains formed on the first and second cell areas;

a connecting area capable of electrically connecting one of the source and drain of

the first cell area with one of the source and drain of the second cell area,

wherein the connecting area has an electric resistance which is lower than any one of the sources and drains of the first and second cell areas.

14. The semiconductor device according to claim 13, wherein a groove is formed on the connecting area on the semiconductor substrate.

15. The semiconductor device according to claim 14, wherein an impurity concentration of the connecting area is the same as an impurity concentration of one of the sources and drains of the first and second cell areas, and is higher than an impurity concentration of the other of the sources and drains of the first and second cell areas.

16. The semiconductor device according to claim 14, wherein the impurity concentration of the connecting area is higher than the impurity concentrations of all the sources and drains of the first and second cell areas.

17. The semiconductor device according to any one of claims 13, wherein at least one part of the connecting area has almost the same impurity depth and almost the same impurity concentration of one of a source/drain area and an off-set area of MOS transistor forming a surrounding circuit of the first and second memory cell areas.

18. A circuit substrate equipped with the semiconductor device according to claim 13.

19. An electronic device comprising a circuit substrate according to claim 18.

20. A method for manufacturing a semiconductor device, comprising:

forming first and second field effect transistors, each having source/drain regions;

forming a conducting region connecting a source/drain region of the first field effect transistor to a source/drain region of the second field effect transistor so that the conducting region has a lower resistance than at least one of the source/drain regions.

21. The method of claim 20, wherein the first and second field effect transistors are formed on a substrate, and further comprising forming a groove between the first and second field effect transistors in the substrate, wherein the groove defines an upper portion of the conducting region.

22. The method of claim 20, wherein the conducting region is formed using a first ion implantation step and at least one of the source/drain regions is formed using a second ion implantation step carried out after the first ion implantation step.

23. The method of claim 20, wherein the conducting region is formed using a first implantation step and the source/drain regions are formed using a second implantation step carried out after the first implantation step, and the first implantation step is carried out using a higher energy than the second implantation step.

24. The method of claim 20, wherein the conducting region has a lower resistance than any of the source/drain regions.

25. The method of claim 20, wherein first and second field effect transistors are each formed to include a floating gate.

26. A semiconductor device comprising:

first and second field effect transistors, each having source/drain regions;

a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second field effect transistor, the conducting region having a lower resistance than at least one of the source/drain regions.

27. A semiconductor device as in claim 26, wherein the device includes a substrate including a groove between at least a portion of the first and second field effect transistors, the groove defining an upper region of the conducting region.

28. The method of claim 27, wherein the conducting region has a lower resistance than any of the source/drain regions.

29. A semiconductor device comprising:

first and second memory cell means for storing data, the first and second memory cell means including source/drain regions;

connecting means for electrically connecting the first and second memory cell means, the connecting means having a resistance lower than that of the source/drain regions.